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Agenda

• Intel® Xeon® Scalable Processor Overview, Platform Features
• Skylake-SP CPU Architecture
• Performance Summary

Content Acknowledgement
• Akhilesh Kumar, Skylake-SP CPU Architect
• Malay Trivedi, Lewisburg PCH Architect
Intel® Xeon® Processor Roadmap

**Intel® Xeon® Processor E7**
Targeted at mission critical applications that value a scale-up system with leadership memory capacity and advanced RAS

**Intel® Xeon® Processor E5**
Targeted at a wide variety of applications that value a balanced system with leadership performance/watt/$

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For more complete information about compiler optimizations, see our Optimization Notice.*
Intel® Xeon® Scalable Processor Feature Overview

**Feature** | **Details**
---|---
Socket | Socket P
Scalability | 2S, 4S, 8S, and >8S (with node controller support)
CPU TDP | 70W – 205W
Chipset | Intel® C620 Series (code name Lewisburg)
Networking | Intel® Omni-Path Fabric (integrated or discrete) 4x10GbE (integrated w/ chipset) 100G/40G/25G discrete options
Compression and Crypto Acceleration | Intel® QuickAssist Technology to support 100Gb/s comp/decomp/crypto 100K RSA2K public key
Storage | Integrated QuickData Technology, VMD, and NTB Intel® Optane™ SSD, Intel® 3D-NAND NVMe & SATA SSD
Security | CPU enhancements (MBE, PPK, MPX) Manageability Engine Intel® Platform Trust Technology Intel® Key Protection Technology
Manageability | Innovation Engine (IE) Intel® Node Manager Intel® Datacenter Manager

**Diagram Details**
- **Skylake-SP CPU**
  - OPA
  - 1x 100Gb OPA Fabric
  - DMI
  - DDR4 2666
- **Lewisburg PCH**
  - Intel® QAT
  - ME
  - IE
  - High Speed IO
  - USB3
  - PCIe3
  - SATA3
  - 10GbE NIC
  - BMC
  - SPI
  - Firmware
  - TP
  - SPI/LPC
- **BMC:** Baseboard Management Controller
- **PCH:** Intel® Platform Controller Hub
- **IE:** Innovation Engine
- **Intel® OPA:** Intel® Omni-Path Architecture
- **Intel® QAT:** Intel® QuickAssist Technology
- **ME:** Manageability Engine
- **NIC:** Network Interface Controller
- **VMD:** Volume Management Device
- **NTB:** Non-Transparent Bridge

**Feature Details**
- **Socket Scalability:** 2S, 4S, 8S, and >8S (with node controller support)
- **CPU TDP:** 70W – 205W
- **Chipset:** Intel® C620 Series (code name Lewisburg)
- **Networking:** Intel® Omni-Path Fabric (integrated or discrete) 4x10GbE (integrated w/ chipset) 100G/40G/25G discrete options
- **Compression and Crypto Acceleration:** Intel® QuickAssist Technology to support 100Gb/s comp/decomp/crypto 100K RSA2K public key
- **Storage:** Integrated QuickData Technology, VMD, and NTB Intel® Optane™ SSD, Intel® 3D-NAND NVMe & SATA SSD
- **Security:** CPU enhancements (MBE, PPK, MPX) Manageability Engine Intel® Platform Trust Technology Intel® Key Protection Technology
- **Manageability:** Innovation Engine (IE) Intel® Node Manager Intel® Datacenter Manager

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Platform Topologies

2S Configurations

4S Configurations

8S Configuration

INTEL® XEON® SCALABLE PROCESSOR SUPPORTS CONFIGURATIONS RANGING FROM 2S-2UPI TO 8S

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Intel® Xeon® Scalable Processor
Re-architected from the Ground Up

- Skylake core microarchitecture, with data center specific enhancements
- Intel® AVX-512 with 32 DP flops per core
- Data center optimized cache hierarchy – 1MB L2 per core, non-inclusive L3
- New mesh interconnect architecture
- Enhanced memory subsystem
- Modular IO with integrated devices
- New Intel® Ultra Path Interconnect (Intel® UPI)
- Intel® Speed Shift Technology
- Security & Virtualization enhancements (MBE, PPK, MPX)
- Optional Integrated Intel® Omni-Path Fabric (Intel® OPA)

<table>
<thead>
<tr>
<th>Features</th>
<th>Intel® Xeon® Processor E5-2600 v4</th>
<th>Intel® Xeon® Scalable Processor</th>
</tr>
</thead>
<tbody>
<tr>
<td>Cores Per Socket</td>
<td>Up to 22</td>
<td>Up to 28</td>
</tr>
<tr>
<td>Threads Per Socket</td>
<td>Up to 44 threads</td>
<td>Up to 56 threads</td>
</tr>
<tr>
<td>Last-level Cache (LLC)</td>
<td>Up to 55 MB</td>
<td>Up to 38.5 MB (non-inclusive)</td>
</tr>
<tr>
<td>QPI/UPI Speed (GT/s)</td>
<td>2x QPI channels @ 9.6 GT/s</td>
<td>Up to 3x UPI @ 10.4 GT/s</td>
</tr>
<tr>
<td>PCIe® Lanes/Controllers/Speed(GT/s)</td>
<td>40 / 10 / PCIe® 3.0 (2.5, 5, 8 GT/s)</td>
<td>48 / 12 / PCIe 3.0 (2.5, 5, 8 GT/s)</td>
</tr>
<tr>
<td>Memory Population</td>
<td>4 channels of up to 3 RDIMMs, LRDIMMs, or 3DS LRDIMMs</td>
<td>6 channels of up to 2 RDIMMs, LRDIMMs, or 3DS LRDIMMs</td>
</tr>
<tr>
<td>Max Memory Speed</td>
<td>Up to 2400</td>
<td>Up to 2666</td>
</tr>
<tr>
<td>TDP (W)</td>
<td>55W-145W</td>
<td>70W-205W</td>
</tr>
</tbody>
</table>

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Core Microarchitecture Enhancements

- Larger and improved branch predictor, higher throughput decoder, larger window to extract ILP
- Improved scheduler and execution engine, improved throughput and latency of divide/sqrt
- More load/store bandwidth, deeper load/store buffers, improved prefetcher
- Data center specific enhancements: Intel® AVX-512 with 2 FMAs per core, larger 1MB MLC

ABOUT 10% PERFORMANCE IMPROVEMENT PER CORE ON INTEGER APPLICATIONS AT SAME FREQUENCY
Intel® Advanced Vector Extensions 512 (Intel® AVX-512)

- 512-bit wide vectors
- 32 operand registers
- 8 64b mask registers
- Embedded broadcast
- Embedded rounding

<table>
<thead>
<tr>
<th>Microarchitecture</th>
<th>Instruction Set</th>
<th>SP FLOPs / cycle</th>
<th>DP FLOPs / cycle</th>
</tr>
</thead>
<tbody>
<tr>
<td>Skylake</td>
<td>Intel® AVX-512 &amp; FMA</td>
<td>64</td>
<td>32</td>
</tr>
<tr>
<td>Haswell / Broadwell</td>
<td>Intel AVX2 &amp; FMA</td>
<td>32</td>
<td>16</td>
</tr>
<tr>
<td>Sandybridge</td>
<td>Intel AVX (256b)</td>
<td>16</td>
<td>8</td>
</tr>
<tr>
<td>Nehalem</td>
<td>SSE (128b)</td>
<td>8</td>
<td>4</td>
</tr>
</tbody>
</table>

**Intel AVX-512 Instruction Types**

- **AVX-512-F**: AVX-512 Foundation Instructions
- **AVX-512-VL**: Vector Length Orthogonality: ability to operate on sub-512 vector sizes
- **AVX-512-BW**: 512-bit Byte/Word support
- **AVX-512-DQ**: Additional D/Q/SP/DP instructions (converts, transcendental support, etc.)
- **AVX-512-CD**: Conflict Detect: used in vectorizing loops with potential address conflicts

**POWERFUL INSTRUCTION SET FOR DATA-PARALLEL COMPUTATION**

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Performance and Efficiency with Intel® AVX-512

INTEL® AVX-512 DELIVERS SIGNIFICANT PERFORMANCE AND EFFICIENCY GAINS

Source as of June 2017: Intel internal measurements on platform with Xeon Platinum 8180, Turbo enabled, UPI=10.4, SNC1, 6x32GB DDR4-2666 per CPU, 1 DPC. Software and workloads used in performance tests may have been optimized for performance only on Intel microprocessors. Performance tests, such as SYSmark and MobileMark, are measured using specific computer systems, components, software, operations and functions. Any change to any of those factors may cause the results to vary. You should consult other information and performance tests to assist you in fully evaluating your contemplated purchases, including the performance of that product when combined with other products.

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New Mesh Interconnect Architecture

Broadwell EX 24-core die

- SKX Core
- SKX Core
- SKX Core
- SKX Core
- CBO
- CBO
- CBO
- CBO
- DDR
- DDR
- DDR
- DDR
- PCIe x16
- PCIe x8
- PCIe x4 (ESI)
- UBox PCU
- Home Agent
- DDR Mem Ctlr
- DDR Mem Ctlr
- DDR Mem Ctlr
- DDR Mem Ctlr

Skylake-SP 28-core die

- SKX Core
- SKX Core
- SKX Core
- SKX Core
- CBO
- CBO
- CBO
- CBO
- DDR
- DDR
- DDR
- DDR
- PCIe x16
- PCIe x16
- PCIe x16
- On Pkg PCIe x16
- 1x UPI x20
- 2x UPI x20

- CHA/SP/LLC
- CHA/SP/LLC
- CHA/SP/LLC
- CHA/SP/LLC
- CHA/SP/LLC
- CHA/SP/LLC
- CHA/SP/LLC
- CHA/SP/LLC
- CHA/SP/LLC
- CHA/SP/LLC
- CHA/SP/LLC
- CHA/SP/LLC
- SKX Core
- SKX Core
- SKX Core
- SKX Core
- SKX Core
- SKX Core
- SKX Core
- SKX Core
- SKX Core
- SKX Core
- SKX Core
- SKX Core

CHA – Caching and Home Agent; SF – Snoop Filter; LLC – Last Level Cache; SKX Core – Skylake Server Core; UPI – Intel® UltraPath Interconnect

MESH IMPROVES SCALABILITY WITH HIGHER BANDWIDTH AND REDUCED LATENCIES

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Re-Architected L2 & L3 Cache Hierarchy

**Previous Architectures**

- **Shared L3**
  - 2.5MB/core (inclusive)

  - L2 (256KB private)
  - L2 (256KB private)
  - L2 (256KB private)

**Core**

**Skylake-SP Architecture**

- **Shared L3**
  - 1.375MB/core (non-inclusive)

  - L2 (1MB private)
  - L2 (1MB private)
  - L2 (1MB private)

**Core**

- On-chip cache balance shifted from shared-distributed (prior architectures) to private-local (Skylake architecture):
  - Shared-distributed ➔ shared-distributed L3 is primary cache
  - Private-local ➔ private L2 becomes primary cache with shared L3 used as overflow cache

- Shared L3 changed from inclusive to non-inclusive:
  - Inclusive (prior architectures) ➔ L3 has copies of all lines in L2
  - Non-inclusive (Skylake architecture) ➔ lines in L2 *may not* exist in L3

**SKYLAKE-SP CACHE HIERARCHY ARCHITECTED SPECIFICALLY FOR DATA CENTER USE CASE**
Memory Subsystem

2 Memory Controllers, 3 channels each ➔ total of 6 memory channels

- DDR4 up to 2666, 2 DIMMs per channel
- Support for RDIMM, LRDIMM, and 3DS-LRDIMM
- 1.5TB Max Memory Capacity per Socket (2 DPC with 128GB DIMMs)
- >60% increase in Memory BW per Socket compared to Intel® Xeon® processor E5 v4

Supports XPT prefetch to reduce LLC miss latency
Introduces a new memory device failure detection and recovery scheme with Adaptive Double Device Data Correction (ADDDC)

**SIGNIFICANT MEMORY BANDWIDTH AND CAPACITY IMPROVEMENTS**
Memory Performance
Bandwidth-Latency Profile

Source as of June 2017: Intel internal measurements on platform with Xeon Platinum 8180, Turbo enabled, UPI=10.4, SNC1/SNC2, 6x32GB DDR4-2400/2666 per CPU, 1 DPC, and platform with E5-2699 v4, Turbo enabled, 4x32GB DDR4-2400, RHEL 7.0. Software and workloads used in performance tests may have been optimized for performance only on Intel microprocessors. Performance tests, such as SYSmark and MobileMark, are measured using specific computer systems, components, software, operations and functions. Any change to any of those factors may cause the results to vary. You should consult other information and performance tests to assist you in fully evaluating your contemplated purchases, including the performance of that product when combined with other products. For more information go to [http://www.intel.com/performance](http://www.intel.com/performance).
1.65x Average\(^1\) Generational Gains on 2-Socket Servers with Intel® Xeon® Scalable Processor

Higher is better

<table>
<thead>
<tr>
<th>Test</th>
<th>Relative 2S Performance</th>
</tr>
</thead>
<tbody>
<tr>
<td>1-node 2x Intel® Xeon® processor E5-26xx v4 (&quot;Broadwell-EP 2S&quot;)</td>
<td>1.65x Average</td>
</tr>
<tr>
<td>1-node 2x Intel® Xeon® Scalable processor</td>
<td>2.27</td>
</tr>
</tbody>
</table>


Software and workloads used in performance tests may have been optimized for performance only on Intel microprocessors. Performance tests, such as SYSmark and MobileMark, are measured using specific computer systems, components, software, operations and functions. Any change to any of those factors may cause the results to vary. You should consult other information and performance tests to assist you in fully evaluating your contemplated purchases, including the performance of that product when combined with other products. For more information go to Intel’s Performance tests site. Intel does not control or audit the design or implementation of third party benchmark data or Web sites referenced in this document. Intel encourages all of its customers to visit the referenced Web sites or others where similar performance benchmark data are reported and confirm whether the referenced benchmark data are accurate and reflect performance of systems available for purchase. Configurations: see slides 23, 24. *Other names and brands may be claimed as the property of others.
Monte Carlo European Option increased performance with the 2S Intel® Xeon® Gold 6148 processor

**Application:**
Monte Carlo is a numerical method that uses statistical sampling techniques to approximate solutions to quantitative problems. In finance, Monte Carlo algorithms are used to evaluate complex instruments, portfolios, and investments. This is compute bound, double precision workload.

**Potential Customer Benefits:**
- Higher performance allow either doing the same work faster leading to improved TCO or simulation of more paths leading to higher confidence in results.

**Performance Factors:**
- Using Intel® AVX-512 SIMD vectorization improved performance by 1.85X over Intel® AVX2.
- Higher core counts of Intel Xeon® Gold 6148 processor contributes to higher performance.
- Better memory hierarchy adds to the performance
- Code modernization strategy: Parallelizing outer loop over options and vectorize inner loop of paths.

Software and workloads used in performance tests may have been optimized for performance only on Intel microprocessors. Performance tests, such as SYSmark and MobileMark, are measured using specific computer systems, components, software, operations and functions. Any change to any of those factors may cause the results to vary. You should consult other information and performance tests to assist you in fully evaluating your contemplated purchases, including the performance of that product when combined with other products. For more complete information visit [http://www.intel.com/performance](http://www.intel.com/performance).

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The Secure, Agile, Next-Generation Platform for Multi-Cloud Infrastructures

**Pervasive Performance for Actionable Insights**

- Skylake-SP cores
- Intel® AVX-512
- Feeds: UPI, 6x DDR4, 3x16 PCIe, Intel® SSDs
- Integration: Intel® Ethernet / Omni-Path / Intel® QuickAssist / FPGA

**Security Without Compromise**

- Intel® AVX-512
- PPK, MPX, MBE
- Intel® QAT w/ Secure Key Management
- Intel® Boot Guard
- Intel® Trusted Infrastructure

**Agile Service Delivery**

- Intel® Volume Management Device Technology
- Intel® RAS
- Open Stack Software Optimizations
CODE THAT PERFORMS AND OUTPERFORMS

Download a free, 30-day trial of Intel® Parallel Studio XE 2018 today


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To check your inbox for the evaluation survey which will be emailed after this presentation.

P.S.

Everyone who fills out the survey will receive a personalized certificate indicating completion of the training!
BENCHMARK CONFIGURATION SUMMARY


b) Up to 1.40x on SPECvirt_sc* 2013: Claim based on best-published 2-socket SPECvirt_sc* 2013 result submitted to/published at http://www.spec.org/virt_sc2013/results/res2016q3/virt_sc2013-20160823-00060-perf.html as of 11 July 2017. Score: 2360 @ 137 VMs vs. 1-Node, 2 x Intel® Xeon® Platinum 8180 Processor with 768 GB (24 x 32 GB, 2R x4 PC4-2666 DDR4 2666MHz RDIMM) Total Memory on SUSE Linux Enterprise Server 12 SP2. Data Source: http://www.spec.org, Benchmark: SPECvirt_sc* 2013, Score: 3323 @ 189 VMs Higher is better


g) Up to 1.65x on STREAM - triad: 1-Node, 2 x Intel® Xeon® Processor E5-2699 v4 on Grantley-EP (Wellsburg) with 256 GB Total Memory on Red Hat Enterprise Linux* 6.5 kernel 2.6.32-431 using Stream NTW avx2 measurements. Data Source: Request Number: 1709, Benchmark: STREAM - Triad, Score: 127.7 Higher is better vs. 1-Node, 2 x Intel® Xeon® Platinum 8180 Processor on Neon City with 384 GB Total Memory on Red Hat Enterprise Linux* 7.2-kernel 3.10.0-327 using STREAM AVX 512 Binaries. Data Source: Request Number: 2500, Benchmark: STREAM - Triad, Score: 199 Higher is better
Up to 1.73x on HammerDB: 1-Node, 2 x Intel® Xeon® Processor E5-2699 v4 on Grantley-EP (Wellsburg) with 384 GB Total Memory on Red Hat Enterprise Linux® 7.1 kernel 3.10.0-229 using Oracle 12.1.0.2.0 (including database and grid) with 800 warehouses, HammerDB 2.18. Data Source: Request Number: 1645, Benchmark: HammerDB, Score: 4.13568e+006 Higher is better vs. 1-Node, 2 x Intel® Xeon® Platinum 8180 Processor on Purley-EP (Lewisburg) with 768 GB Total Memory on Oracle Linux® 7.2 using Oracle 12.1.0.2.0, HammerDB 2.18. Data Source: Request Number: 2510, Benchmark: HammerDB, Score: 7.18049e+006 Higher is better

LAMMPS is a classical molecular dynamics code, and an acronym for Large-scale Atomic/Molecular Massively Parallel Simulator. It is used to simulate the movement of atoms to develop better therapeutics, improve alternative energy devices, develop new materials, and more. E5-2697 v4: 2S Intel® Xeon® processor E5-2697 v4, 2.3GHz, 36 cores, Intel® Turbo Boost Technology and Intel® Hyperthreading Technology on, BIOS 86B0271.R00, 8x16GB 2400MHz DDR4, Red Hat Enterprise Linux® 7.2 kernel 3.10.0-327. Gold 6148: 2S Intel® Xeon® Gold 6148 processor, 2.4GHz, 40 cores, Intel® Turbo Boost Technology and Intel® Hyperthreading Technology on, BIOS 86B.01.00.0412.R00, 12x16GB 2666MHz DDR4, Red Hat Enterprise Linux® 7.2 kernel 3.10.0-327.


Up to 1.87x on Black-Scholes: which is a popular mathematical model used in finance for European option valuation. This is a double precision version. E5-2697 v4: 2S Intel® Xeon® processor CPU E5-2697 v4 , 2.3GHz, 36 cores, turbo and HT on, BIOS 86B0271.R00, 128GB total memory, 8 x16GB 2400 MHz DDR4 RDIMM, 1 x 1TB SATA, Red Hat Enterprise Linux® 7.2 kernel 3.10.0-327. Gold 6148: Intel® Xeon® Gold processor 6148@ 2.4GHz, H0QS, 40 cores 150W. QMS1, turbo and HT on, BIOS SESC620.06B.01.00.0412.02092017z159, 192GB total memory, 12 x 16 GB 2666 MHz DDR4 RDIMM, 1 x 800GB INTEL SSD SC2BA80, Red Hat Enterprise Linux® 7.2 kernel 3.10.0-327

Up to 2.27x on LINPACK*: 1-Node, 2 x Intel® Xeon® Processor E5-2699 v4 on Grantley-EP (Wellsburg) with 64 GB Total Memory on Red Hat Enterprise Linux® 7.0 kernel 3.10.0-123 using MP_LINPACK 11.3.1 (Composer XE 2016 U1). Data Source: Request Number: 1636, Benchmark: Intel® Distribution of LINPACK, Score: 1446.4 Higher is better vs. 1-Node, 2 x Intel® Xeon® Platinum 8180 Processor on Wolf Pass SKX with 384 GB Total Memory on Red Hat Enterprise Linux® 7.3 using mp_lapack_2017.1.013. Data Source: Request Number: 3753, Benchmark: Intel® Distribution of LINPACK, Score: 3295.57 Higher is better
Monte Carlo Benchmark Configuration Summary

Monte Carlo – Testing conducted on Monte Carlo software comparing 2S Intel® Xeon® Gold 6148 processor to 2S Intel® Xeon® Processor E5-2697 v3 and to 2S Intel® Xeon® Processor E5-2697 v4. OS: Red Hat Enterprise Linux® 7.2 kernel 3.10.0-327. Testing by Intel March 2017. BASELINE: 2S Intel® Xeon® processor E5-2697 v3, 2.6GHz, 28 cores, turbo and HT on, BIOS 86B.0036.R05, 64GB total memory, 8x8GB 2133 MHz DDR4, Fedora release 20 kernel 3.15.10-200. NEXT GEN: 2S Intel® Xeon® processor E5-2697 v4, 2.3GHz, 36 cores, turbo and HT on, BIOS 86B0271.R00, 128GB total memory, 8 x16GB 2400 MHz DDR4 RDIMM, 1 x 1TB SATA, Red Hat Enterprise Linux® 7.2 kernel 3.10.0-327. NEW: 2S Intel® Xeon® Gold 6148 processor @ 2.4GHz, H0QS, 40 cores 150W, QMS1, turbo and HT on, BIOS SE5C620.86B.01.00.0412.020920172159, 192GB total memory, 12 x 16 GB 2666 MHz DDR4 RDIMM, 1 x 800GB Intel® SSD SC2BA80, Red Hat Enterprise Linux® 7.2 kernel 3.10.0-327.